REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1 – 10 are pending in this application. Claims 1 and 8 stand rejected. Claims 2 - 7, 9 and 10 have been allowed. No new matter has been added. The rejections set forth in the Office Action are respectfully traversed below.

Objection to the Title

On page 2, item 2 of the Office Action, the title of the invention was objected to for allegedly not being descriptive. The title of the invention has been changed to "A CLOCK SUPPLY CONTROL APPARATUS AND METHOD FOR PCI DEVICES."

Approval and entry of the new title is respectfully requested. However, if the Examiner finds the new title to be objectionable, the Examiner is invited to provide a new title that he finds appropriately descriptive.

In the Drawings

Figures 1 – 3 were objected to for not including a legend - - Prior Art - -. Figures 1, 2 and 3 have been labeled as "Prior Art."

Approval and entry of the changes to the drawings are respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claims 1 and 8 stand rejected under 35 U.S.C. §102(a) as being anticipated by the description of the related art set forth in the Background of the Invention section of the application, referred to the Examiner as "Applicant Admitted Prior Art (AAPA)." For the reasons set forth in detail below, this rejection is respectfully traversed.

The present invention is directed to a computer system that effectively uses a clock run function (provided in order to save consumption power of PCI devices) concurrently with a serialized interrupt processing function of the PCI devices being set in the active condition.

By way of example, current claims 1 and 8 are supported by Figures 4-8 and the corresponding descriptions (page 10, line 12, through page 18, line 14) in the specification. For example the present application discloses a clock supply control apparatus which controls supply of a clock signal to first and second devices (element 69 and elements 65-67 in FIG. 4) of a computer system (element 40 in FIG. 4), comprising a clock generating unit (element 48 in FIGS 4 or element 91 in FIG.) generating a clock signal; a clock supply logic unit (element 96 in FIG. 8) controlling supply of the clock signal from the clock generating unit to the second device in response to a clock control signal, the second device being operable with the clock signal supplied from the clock supply logic unit; and a controller (element 75 in FIGS 5 or element 63 in FIG. 4) setting the clock control signal at one of a clock supply inhibition level and a clock supply allowance level in response to a state of a clock run signal line (element 80 in FIG. 4), the resulting clock control signal being supplied from the controller to the clock supply logic unit

(element 96), wherein the first device (element 69) is operable with the clock signal from the clock generating unit (element 96) and outputs an interrupt signal to an interrupt signal line (element 82 in FIG. 4) regardless of whether the clock control signal (PCI STP) is set at the clock supply inhibition level or the clock supply allowance level. See, for example, application specification at page 17, lines 4-14.

The related art shown in Figures 1-3 and described on pages 1-5 of the application discloses a peripheral component interconnect (PCI) bus controller of a conventional computer system, which requires that the PCI devices 31-1 through 31-n output interrupt signals having a specific pattern to an interrupt signal line 32 at a given timing (see Figure 3). To achieve this requirement, the PCI devices 31-1 through 31-n must be operated in synchronism with a PCI bus clock supplied thereto.

However, in the computer system configured as shown in Figure 3, if the supply of the PCI bus clock to the PCI devices 31-1 through 31-n is inhibited by performing the known clock run function (which is provided to save power consumption of the PCI devices 31-1 through 31-n), the interrupt processing function of the PCI devices 31-1 through 31-n is placed in the *inactive condition* because of the absence of the clock supplied thereto. Therefore, a problem occurs in that the PCMCIA controller in the inactive condition is unable to provide the plug-and-play capability of the PC card through the interrupt processing function. To avoid this problem, in the conventional computer system in which the PCMCIA controller is installed, the clock run function is set in the inactive condition in order to allow the plug-and-play capability of the PC card.

For this reason, in the conventional computer system described above, *the clock run function (which is intended for the saving of the power consumption of PCI devices) cannot suitably be used during the time period in which the interrupt processing function of the PCMCIA controller is active.*

The related art section of the present application does not disclose or suggest a clock supply control apparatus which controls supply of a clock signal to first and second devices of a computer system, wherein the first device is operable with a clock signal from a clock generating unit and *outputs an interrupt signal* to an interrupt signal line *regardless* of whether a clock control signal is set at a clock supply inhibition level or a clock supply allowance level.

As discussed in the related art, on page 5, lines 14- 17, the *interrupt processing* of the PCI devices 31-1 through 31-n is placed in the *inactive condition* because of the absence of a clock supplied thereto. In contrast, the claimed invention outputs an interrupt signal *regardless* of whether a clock signal (controlled by the clock control signal) is inhibited or supplied.

For example, as explained at page 17, lines 25-34 in the written specification, the clock generator 4 in the embodiment of Figures 4-8 always supplies the PCI clock signal (PCI CLKI) to the PCMCIA controller 69. Even when the PC card 81 is attached to the PC card connector 70 during the active condition of the clock run function, the PCI clock signal (PCI CLK1) is constantly supplied to the PCMCIA controller 69. Upon detection of the active-high card attach signal, the PCMCIA controller 69 generates the interrupt signal of the specific pattern and outputs it to the interrupt signal line 82 in accordance with the PC1 clock signal (PCI CLK1).

Therefore, it is possible that the computer system 40 of the present invention effectively use the clock run function in order to provide the consumption power saving for the PCI devices 65, 66 and 67 even when the serialized interrupt processing function of the PCMCIA controller 69 is active.

In view of the above remarks, it is respectfully submitted that claims 1 and 8 distinguish over the cited prior art. Reconsideration and withdrawal of the rejection of claims 1 and 8 under 35 U.S.C. §102(a) are respectfully requested.

CONCLUSION

For the reasons set forth in detail above, it is respectfully submitted that all pending claims are in condition for allowance. An indication of allowability of all pending claims is respectfully requested.

If the Examiner believes that there are any issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

In the event that any fees are due in connection with the filing of this paper, please charge any fees to Deposit Account No. 50-2866.

Respectfully submitted,

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Enclosures: Petition for Extension of Time
Replacement Drawings: Figures 1, 2 and 3
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